FORM PTO/SB/08A/B (10-01) Substitute for PTO-1449A/B **INFORMATION DISCLOSURE** **STATEMENT BY APPLICANT** (use as many sheets as necessary)	**Attorney Docket Number**	**40704/DMC/F179**
	Application Number	09/851,708
	Filing Date	May 8, 2001
	Applicant(s)	Indradeep Ghosh
	Group Art Unit	2133
	Examiner Name	R. Stephen Dildine, Jr.

U.S. PATENT DOCUMENTS				
EXAMINER INITIALS	Cite No.[1]	DOCUMENT NUMBER Number - Kind Code[2] (If Known)	PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE
RSD		5,748,647	05-05-1998	Bhattacharya et al.

FOREIGN PATENT DOCUMENTS					
EXAMINER INITIALS	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6] (✓)

OTHER DOCUMENTS		
EXAMINER INITIALS	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
RSD		European Search Report dated 19 January 2004 for European Application No. EP 01304884.1-2216, Search Report mailed February 23, 2004 (4 pgs.)
RSD		Ghosh et al., "Automatic Test Pattern Generation for Functional RTL Circuits Using Assignment Decision Diagrams," Design Automation Conference, (IEEE CAT. No. 00CH37106), Proceedings 2000 of ACM/IEEE-CAS/EDAC Design Automation Conference, Los Angeles, California, June 5-9, 2000 (p 43-48).
RSD		Jervan et al., "High-Level Test Synthesis With Hierarchical Test Generation," Proceedings '99 17th Norchip Conference, Oslo, Norway, Nov. 8-9, 1999 (p 291-296).
RSD		Ubar et al., "Efficient Hierarchical Approach to Test Generation for Digital Systems," Tallin Technical University Conference Proceeding, 20 March 2000 (p 189-195).
RSD		Vandeventer et al., "Using Binary Decision Diagrams to Speed Up the Test Pattern Generation of Behavioral Circuit Descriptions Written in Hardware Description Languages," Circuits and Systems, 1994 IEEE International Symposium On London, UK, May 30-June 2, 1994 (p 279-282).

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EXAMINER SIGNATURE	R. Stephen Dildine	DATE CONSIDERED	8/6/04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. [3]Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6]Applicant is to place a check mark here if English Language Translation is attached.

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